
ATLAS

DoE Review

May 7, 2002

ATLAS LBNL Group

M. Barnett, A. Ciocio, **D. Costanzo**, *S. Dardin*, K. Einsweiler, **V. Fadeyev**,
J. Freeman, M. Garcia-Sciveres, M. Gilchriese, **F. Goozen**, C. Haber,
I. Hinchliffe, B. Jayatilaka, Y-H. Kim, S. Loken, P. Lujan, *F. McCormack*,
J. Richardson, **A. Saavedra**, M. Shapiro, H. Spieler, G. Trilling,
L. Vacavant, *T. Weber*, *R. Witharm*, L. Zimmerman

Physics Division

E. Anderssen, L. Blanquart, P. Denes, N. Hartman, B. Holmes, *T. Johnson*,
J. Joseph, E. Mandelli, G. Meddeler, A. Ryan, T. Stillwater, **C. Vu**, *J. Wirth*,
G. Zizka

Engineering Division

P. Calafiura, **W. Lavrijsen**, **C. Leggett**, **M. Marino**, **D. Quarrie**, **C. Tull**

NERSC

Physicist **Postdoc** Grad Student Undergraduate **Engineer** *Technician*

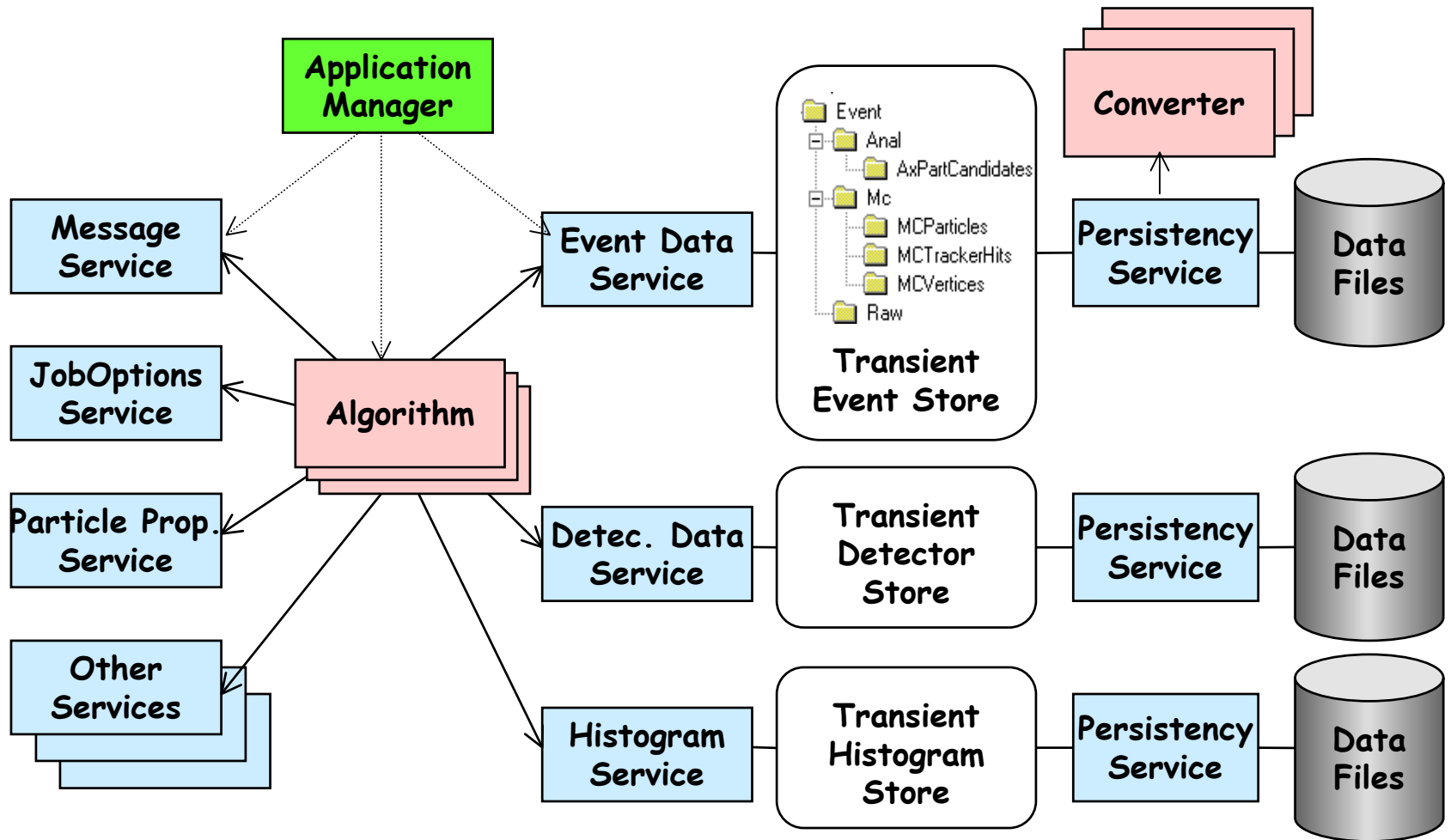
LBNL in ATLAS

- Software, computing and physics simulation
 - Lead role in the development of the Athena framework code(the “operating system” for ATLAS software)
 - Lead role in development and maintenance of physics simulation tools
 - Goal to be Tier 2 site to enable physics analysis
- Silicon strip detector
 - Test system for integrated circuits completed and in operation
 - Module production starting
- Pixel detector
 - Lead roles in electronics and mechanics
 - Production started on mechanical supports and silicon detectors
 - Electronics and module prototypes under test

Software

- D. Quarrie is the ATLAS Chief Architect and member of the Computing Steering Group, responsible for the overall software architecture and planning.
- LBNL personnel are largely responsible for the ATLAS framework code – Athena
 - Athena based on GAUDI developed for LHCb. Some continued joint development with LHCb.
 - Structure in which the user code operates – see diagram next page
 - Provides access to data, histogramming, skeleton for user code.....all of the core functions
 - Everyone must use the framework, and it is now fully accepted within ATLAS(a non-trivial accomplishment)
 - Our work is covered under a signed software agreement(the only one with the U.S. so far)
 - P. Calafiura heads the framework effort.

Athena/GAUDI Architecture



Examples of Current Activity

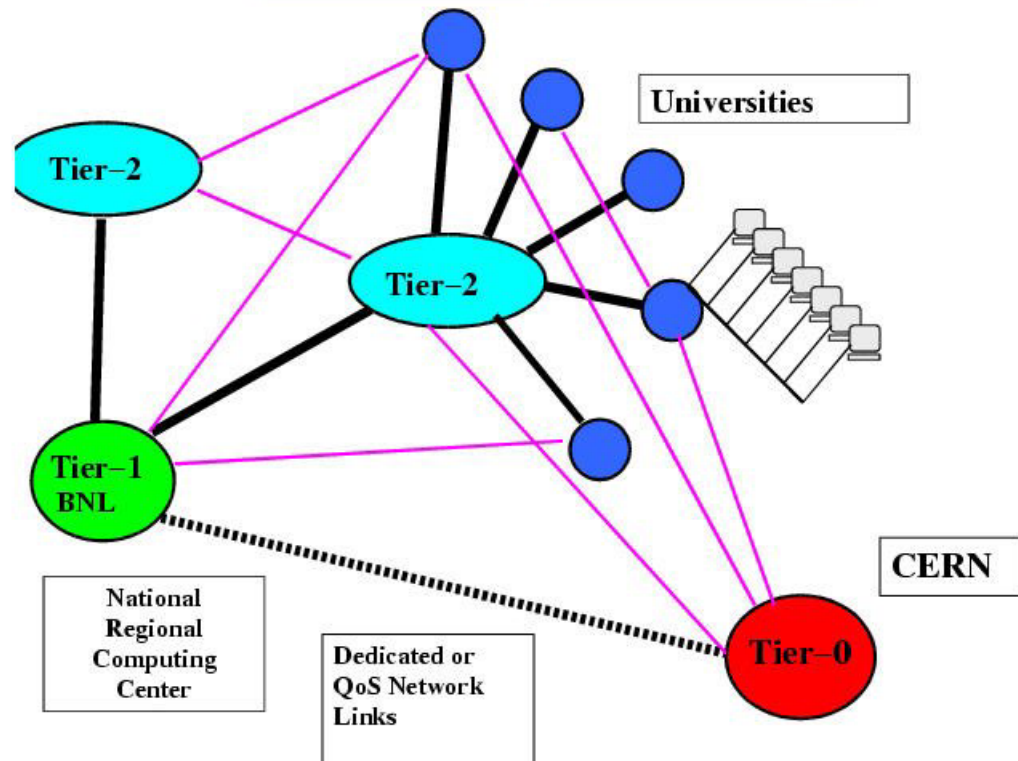
- Support for Pileup(Calafiura, Marino). Read events from multiple streams, combine hits from multiple events in crossing, merge hits in detectors...
- GEANT4 integration into Athena(Leggett). ATLAS had separate simulation framework, now fading after this work.
- Scripting(Lavrisjen). Original GAUDI had no interactive interface, working to implement this eventually with GUI.
- Event Model implementation(Calafiura, Leggett). New event model(what does data look like) needed for next data challenge.
- Conditions database(Calafiura, Leggett). Handles time dependent constant eg. calibrations.
- Detector description(Leggett, Shapiro, Costanzo et al). How the detector is described uniformly for reconstruction and simulation. Old system not maintainable and not same for reconstruction and simulation! Our work will use silicon strips as first example.
- Tutorials(Marino). RealPlayer driven on Web.

Moving to the Data Phase

- Data Challenge(DC)0 is complete. Event generation coordination (Hinchliffe)
- DC1 Part I will begin this month with event generation for the Trigger Technical Design Report
- DC1 Part II will begin by early 2003, will include many physics samples and is intended to begin to exercise the distributed computing system(Grid) that is foreseen during real data taking. A physics workshop to assess the results would follow.
- DC2 would follow in 2004, and would be used to prepare a “Physics Readiness” document.
- It’s likely there will be additional data challenges(or multiple phases)
- I. Hinchliffe is responsible in the U.S. for physics coordination and also has a major role in the overall ATLAS coordination.

Data Analysis Model

- Access to data via grid, world-wide effort underway to make this work.
- Most data analysis (rather than reconstruction and data storage) is foreseen at Tier 2 sites, which also support regional Univs.
- U.S. plan is for 5 Tier 2 sites, with selection starting 2003
- LBNL will seek to be a Tier 2 site, collaborating with NERSC and building on use of PDSF at NERSC by current experiments.
- Current plan – seek NSF support thru campus. Will this work?

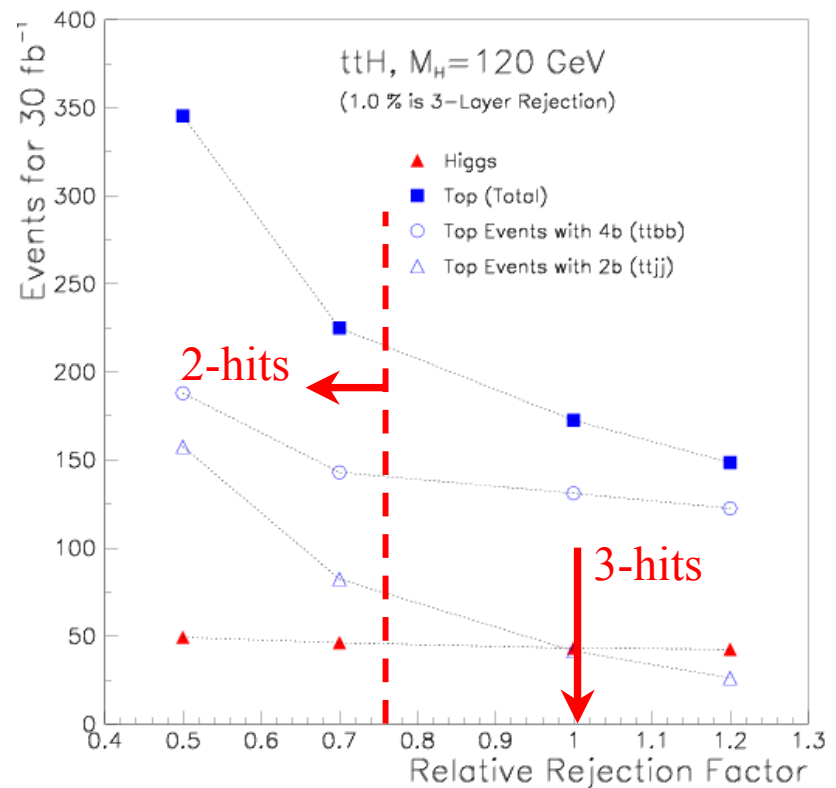


Physics Simulation

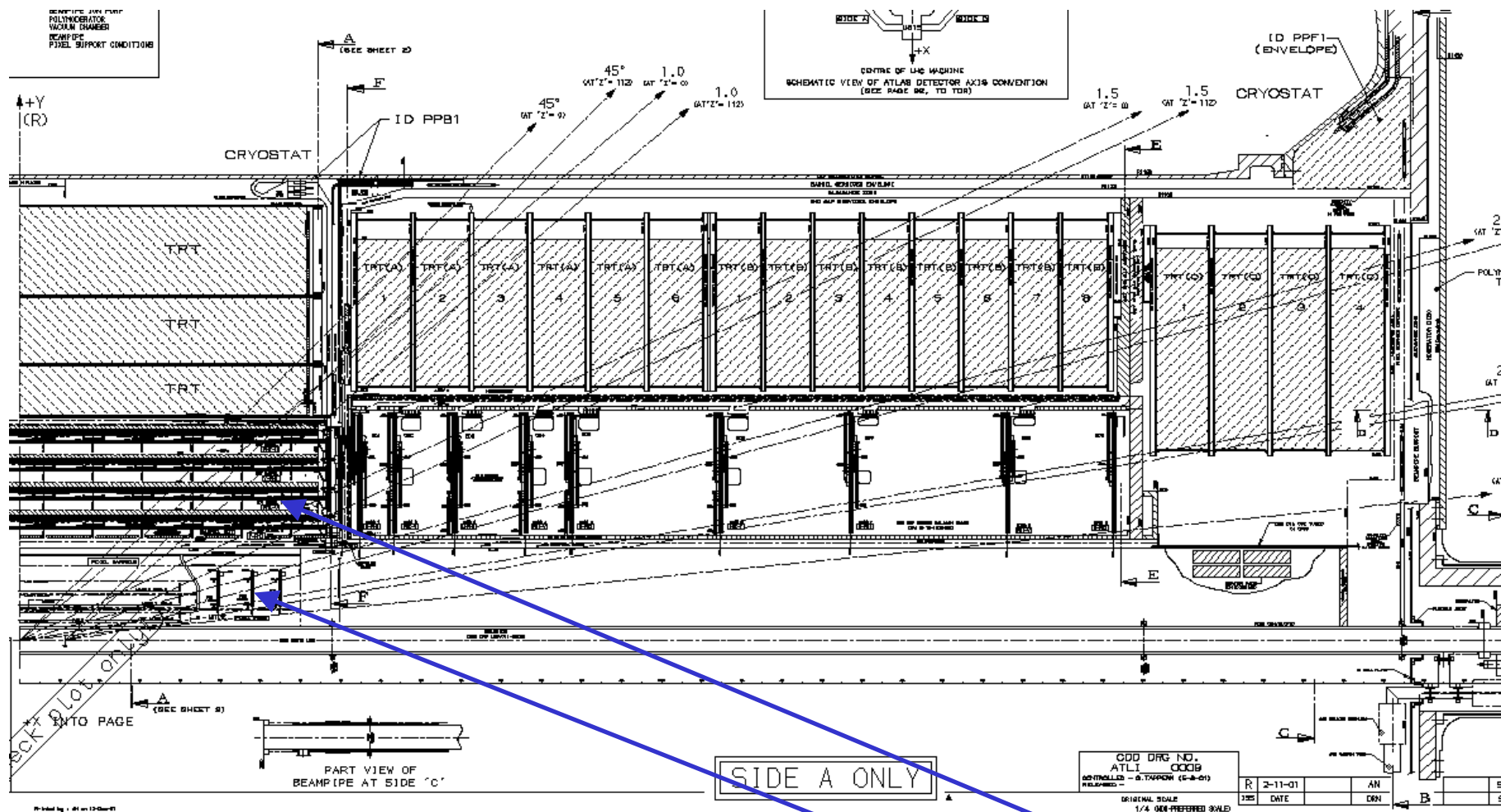
- Studies of signatures for extra dimensions(Vacavant)
- SUSY studies, most recently studies involving τ 's, looking at hadronic decays. Breaking of $e/\mu/\tau$ universality. Helicity of the τ 's carries important information. Full simulation has apparently demonstrated that the helicity can be constrained and that rejection of jet background is sufficient. This work is continuing(Hinchliffe, Vacavant + non-LBNL)
- LHC upgrade studies. Energy and luminosity upgrades, mostly luminosity upgrades(10^{35}). Final report generated. Physics reach improvement interesting, experimental challenges (particularly for tracking) daunting.

Pixel Performance

- Based on simulations done in 1997 and lack of funds, the U.S. long ago decided that the pixel baseline system should have two hits. Our European colleagues have planned on 3 hits until recent LHC budget difficulties.
- LHC delay makes it possible with small incremental cost to add the 3rd hit but we have to make convincing case that performance is improved and we have started detailed simulations.
- Example at right is for 120 GeV Higgs produced with $t\bar{t}$, and Higgs decay into $b\bar{b}$.
- Rejection of jet background depends on pile-up and details of pixel inefficiencies.
- These studies are ongoing, aimed at finalization by Fall this year to make case or not for 3 hits rather than 2.

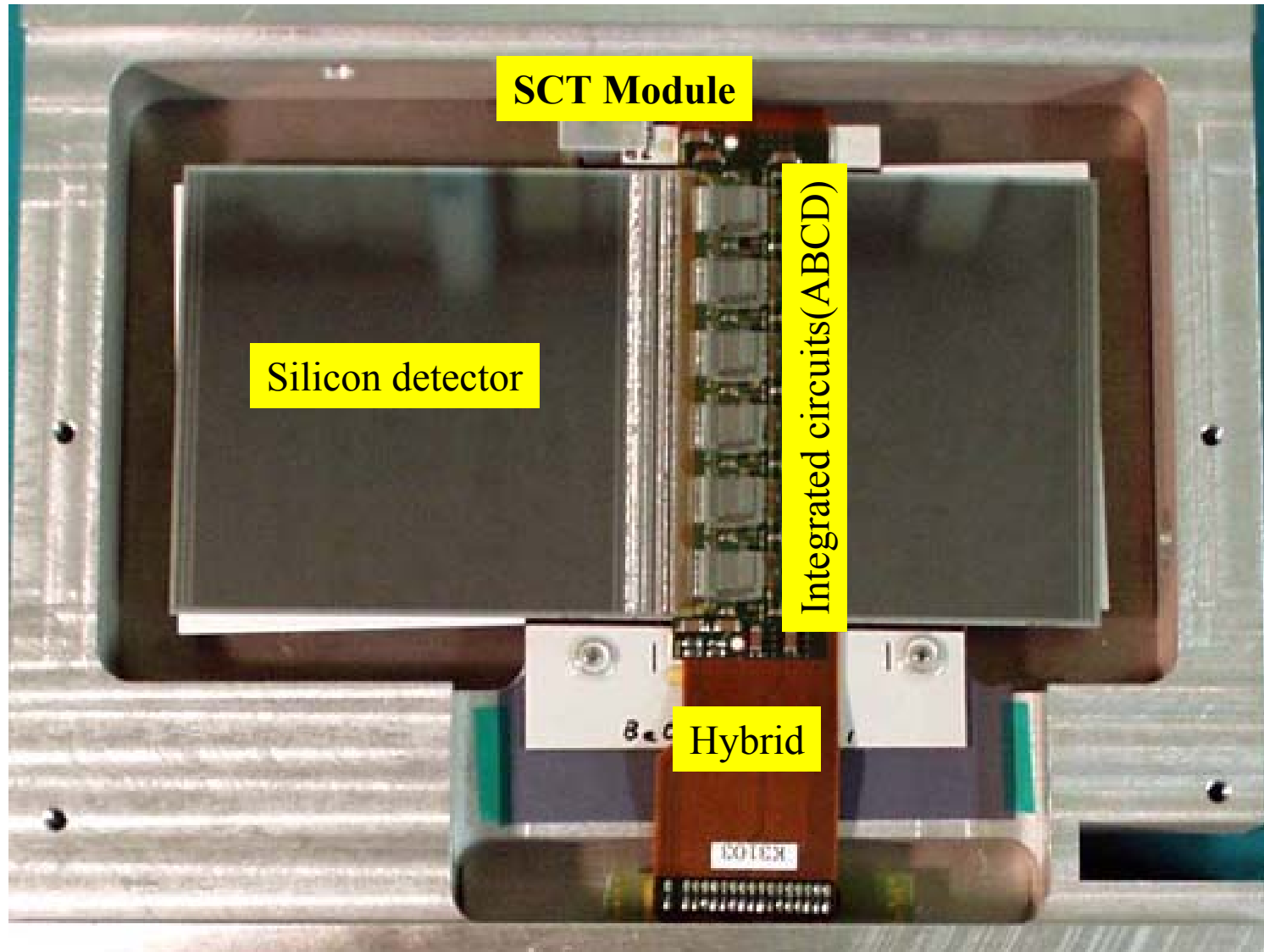


ATLAS Inner Detector



LBNL Technical Roles in Pixels and SCT

Silicon Strip Detector(SCT)



SCT Integrated Circuits

- LBNL designed and built test systems for SCT integrated circuits (ABCDs).
- About 50% of the total ABCD wafers have been fabricated.
- Test systems are now at UCSC(2 stations), RAL(1 station) and CERN(1 station).
- About 30% of the total wafers have been probed. The yield is about 25%, near the contractual minimum(26%).
- Only a few percent of the ICs have been loaded on to hybrids.
- LBNL personnel(Ciocio, Fadeyev, Vu) remain in maintenance mode and to help understand correlations between wafer-probe data and data from hybrids. This will continue until the end of the year.
- We have also completed a low-dose rate irradiation of ICs to over 10 MRad on a hybrid at our Cobalt source to verify chip performance and resolve some issues seen in fast irradiations done at CERN. The chip performance was found to be acceptable, and this was critical to have confidence to proceed to full production(Ciocio, students).

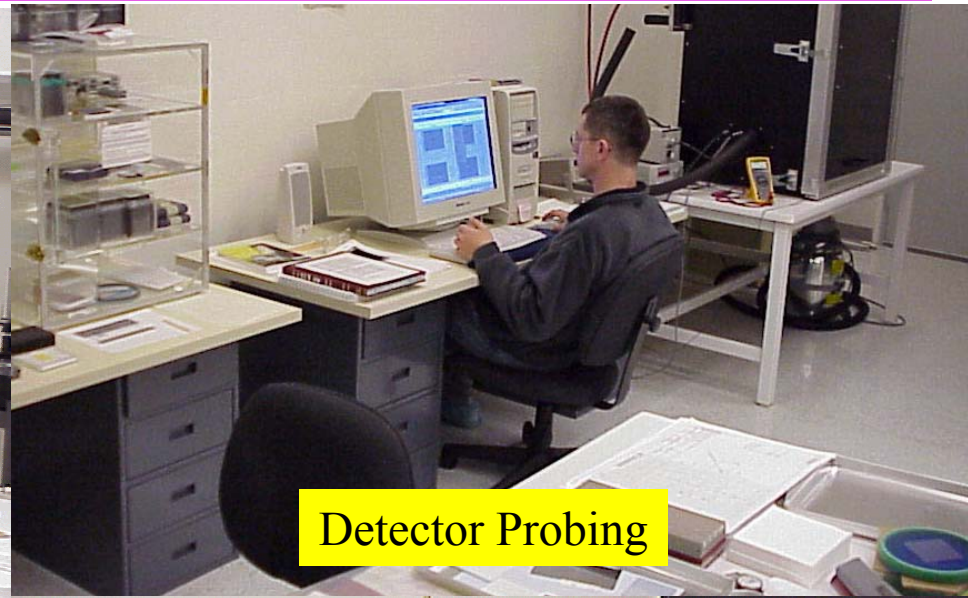
SCT Hybrid&Module Production

- Production facilities in place in clean room in Bldg. 50 for
 - Chip placement on hybrids and wire bonding
 - Detector probing
 - Mechanical module assembly
 - Mechanical metrology(few micron accuracy)
- Facilities for electrical testing of hybrids and modules in place in Bldg. 50
 - Hybrid testing at points in wire bonding sequence
 - After complete assembly of module
 - Burn-in under temperature and humidity control

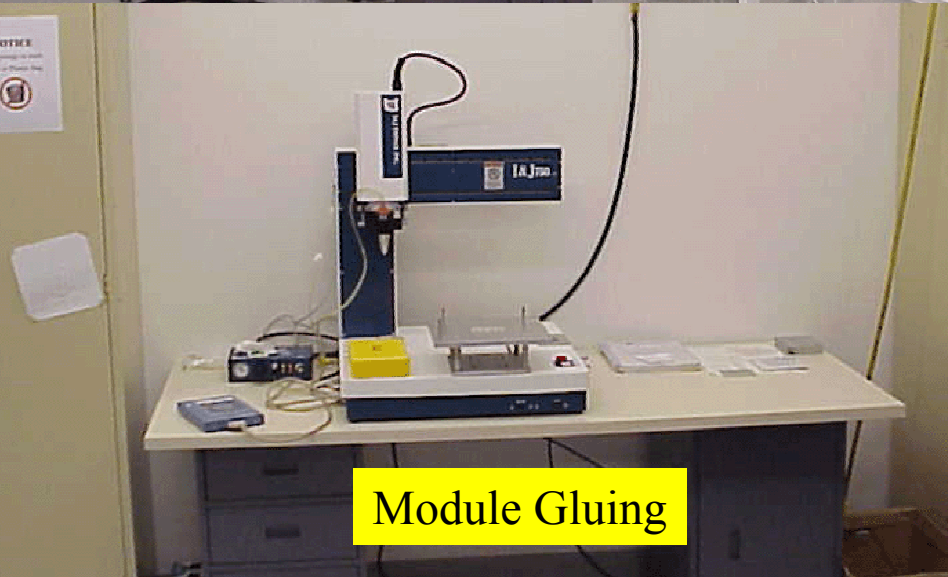
SCT Hybrid/Module Production



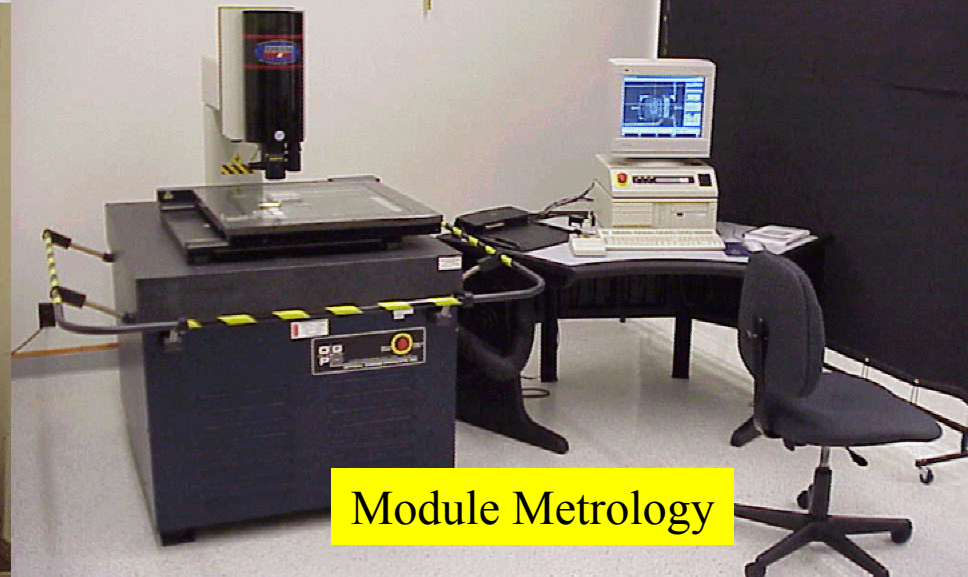
Mechanical Assembly



Detector Probing

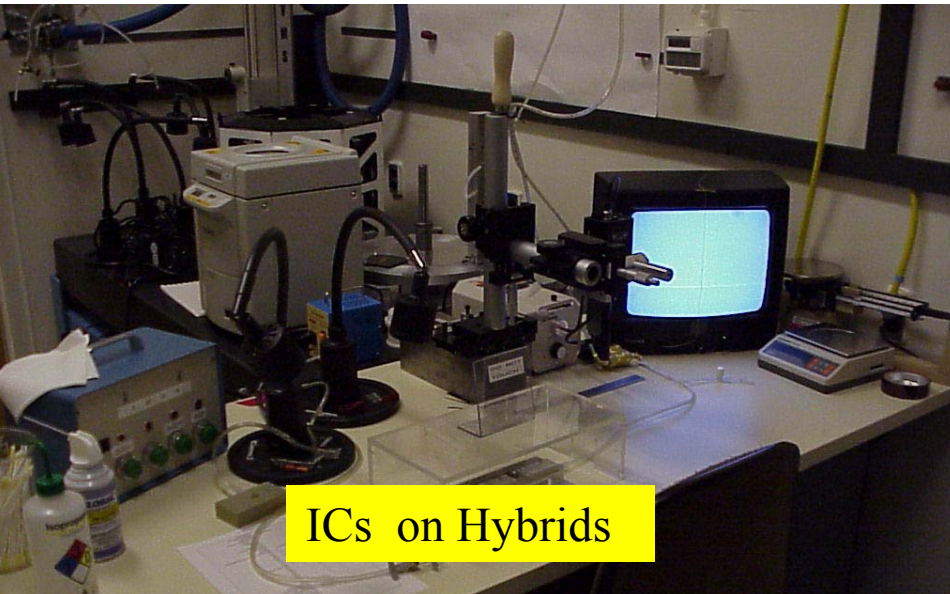


Module Gluing



Module Metrology

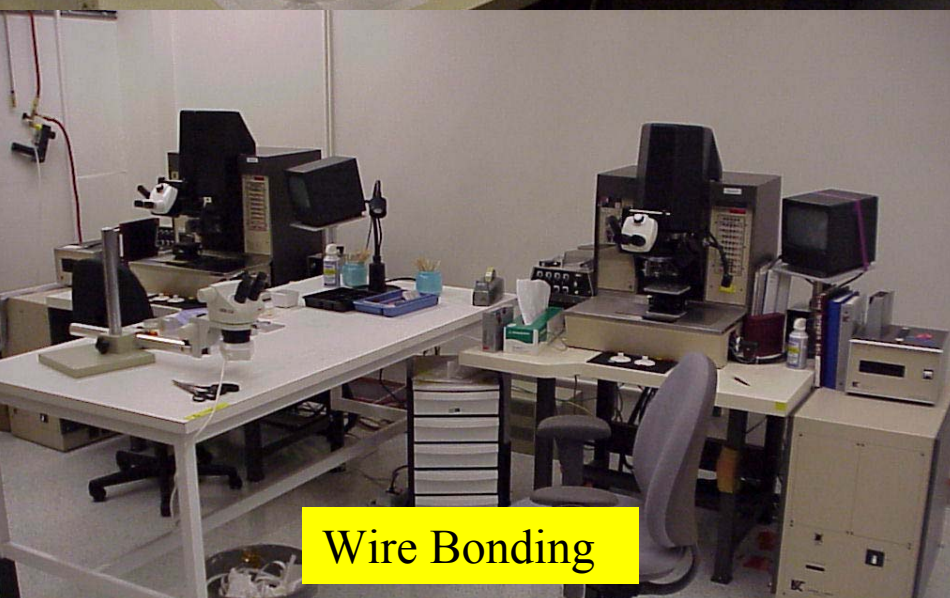
SCT Hybrid/Module Production



ICs on Hybrids



Electrical Testing



Wire Bonding



Electrical Testing

SCT Module Production

- We have built about a dozen dummy modules and have demonstrated that mechanical specs can be met in our facility.
- Four electrical modules have been made and specifications have now been met.
- We are just beginning assembly/testing of five electrical modules with production parts to complete the validation of procedures, to train staff and to demonstrate that we are ready for production.
- Will begin full-production in July when additional tooling sets become available
- Testing capability is nearly complete and will be ready sooner.
- Steady-state production rate is planned to be 3 modules per day by the end of the year.
- The team will be a technical staff of 5 people, 2 of whom are from the Phys. Div.(McCormack, Witharm - bringing some experience from previous silicon projects), engineering(Goozen - experienced in silicon detectors) from Phys. Div., physicists(Haber, Ciocio), post-doc(Fadeyev) and a number of students(primarily involved in testing).
- We are collaborating closely with Santa Cruz on hybrid and module testing and hybrid rework.

Read-Out System

- The SCT(and pixel) systems are read out using VME boards located about 100m from the experiment, on the other end of long fiber optic cables.
- The design and fabrication of all of the boards necessary to read out the SCT and pixel systems is a US responsibility.
- The design work is done by LBNL engineering funded through the University of Wisconsin. Wisconsin supports the effort by having a postdoc resident at LBNL.
- We have bolstered this effort by adding a graduate student, some other student support and some involvement(in the pixel design) by LBNL-supported engineering.
- The final production of the SCT boards is planned for later this year, to be followed afterwards by the pixel boards.

Pixel System

Center Frame Section (1)

Disk Section (2)

Disk
sectors (8)

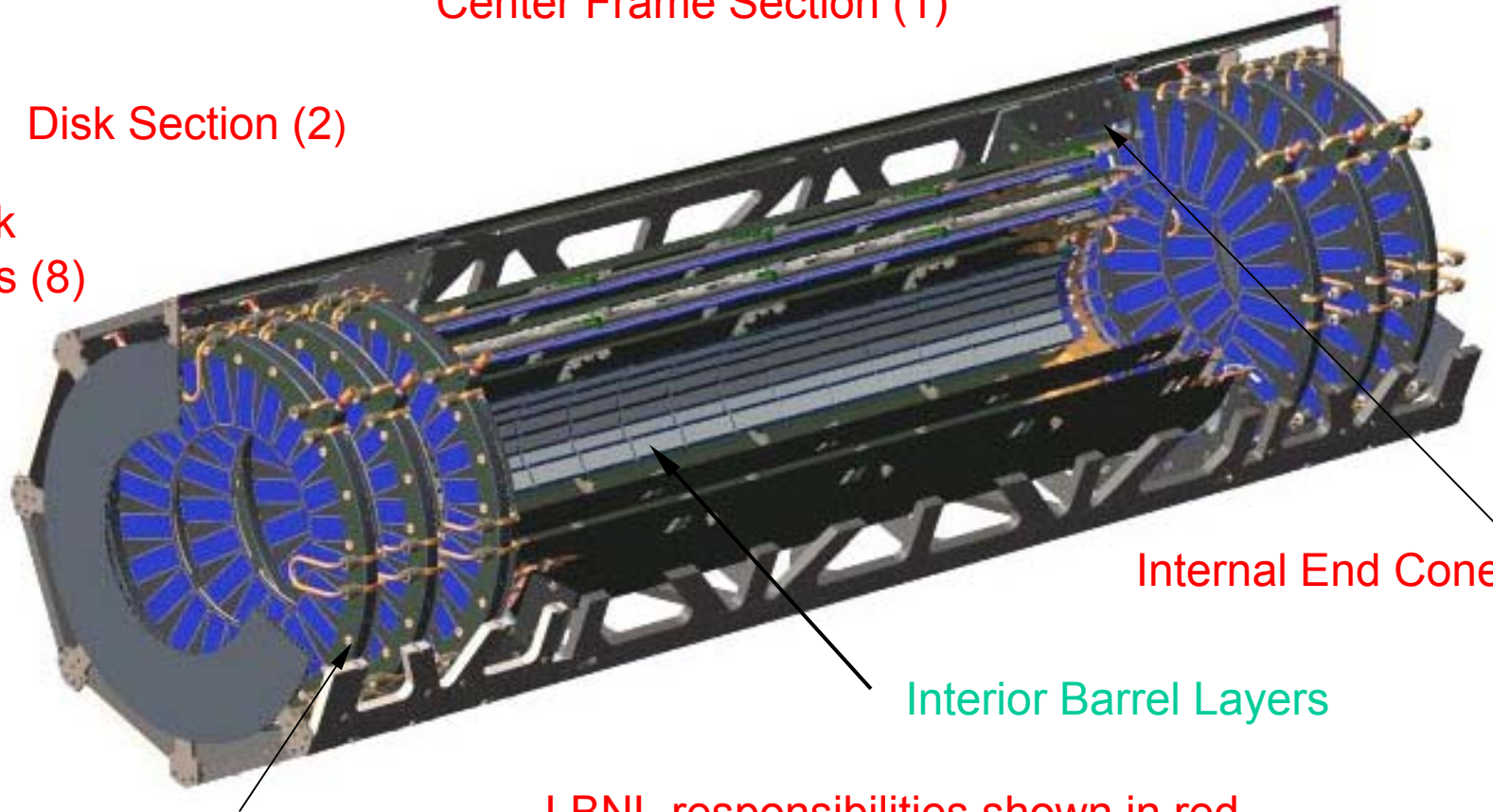
Internal End Cone (2)

Interior Barrel Layers

Disk Rings

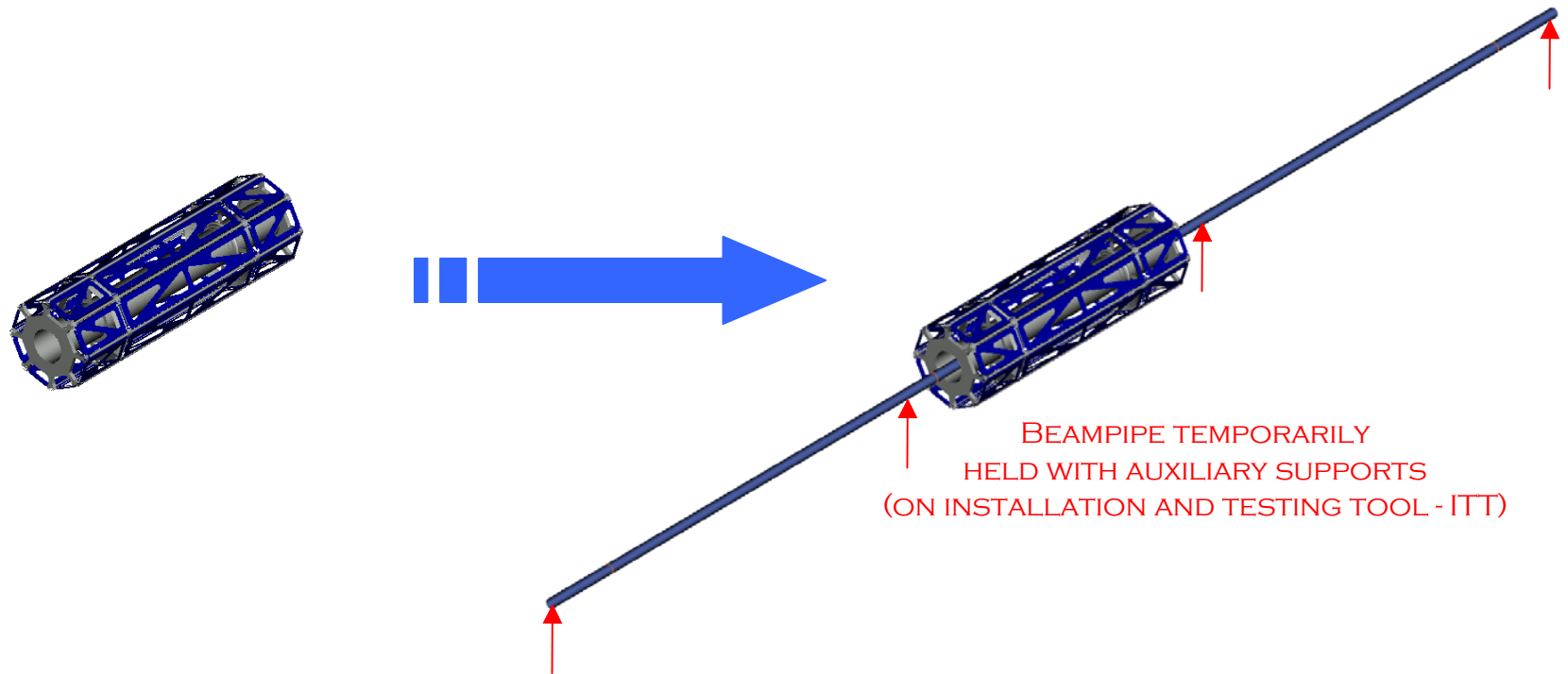
LBL responsibilities shown in red
(Services not shown)

Pixel Size is 50x400 microns

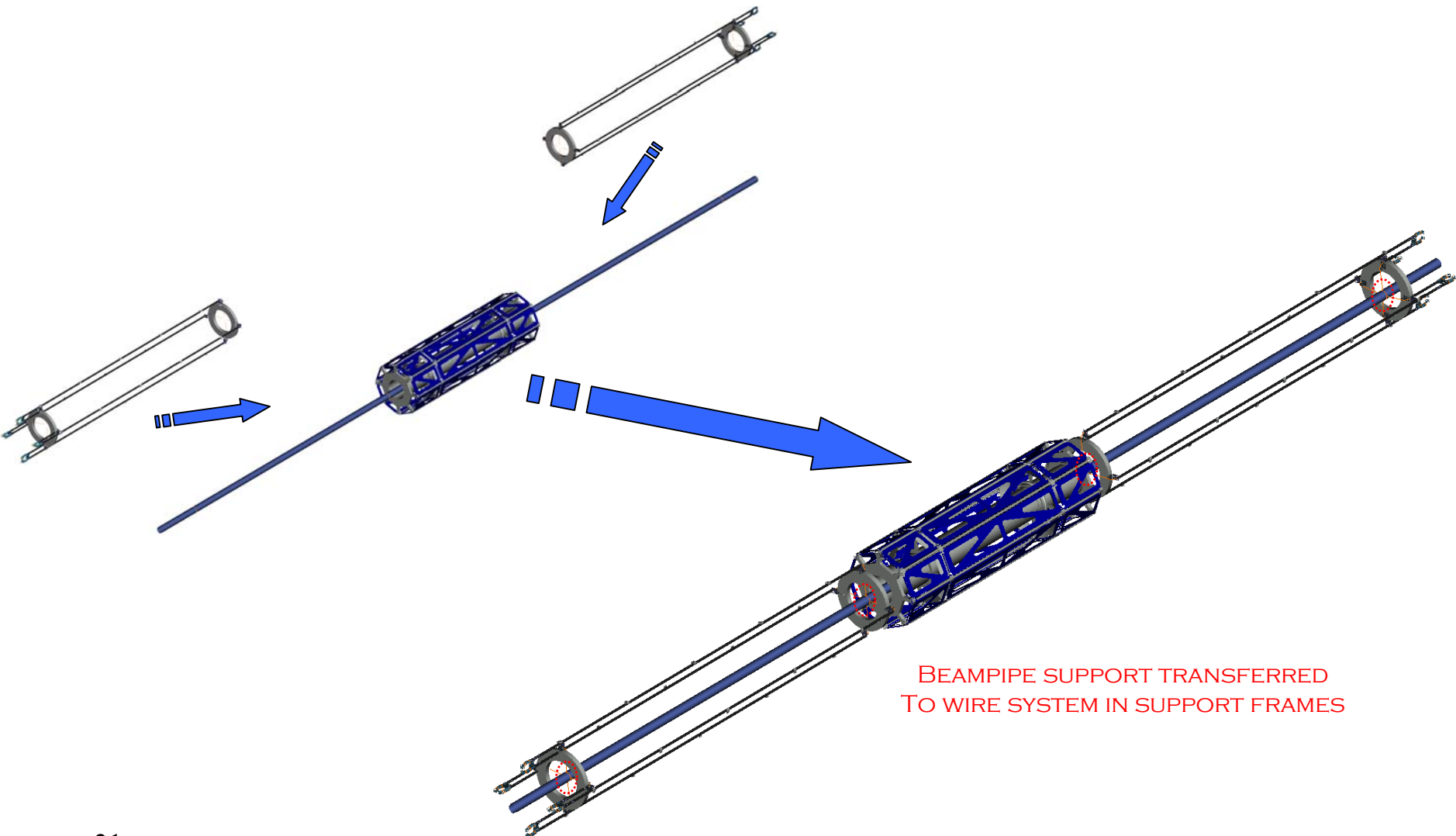


Pixel and Beam Pipe Assembly

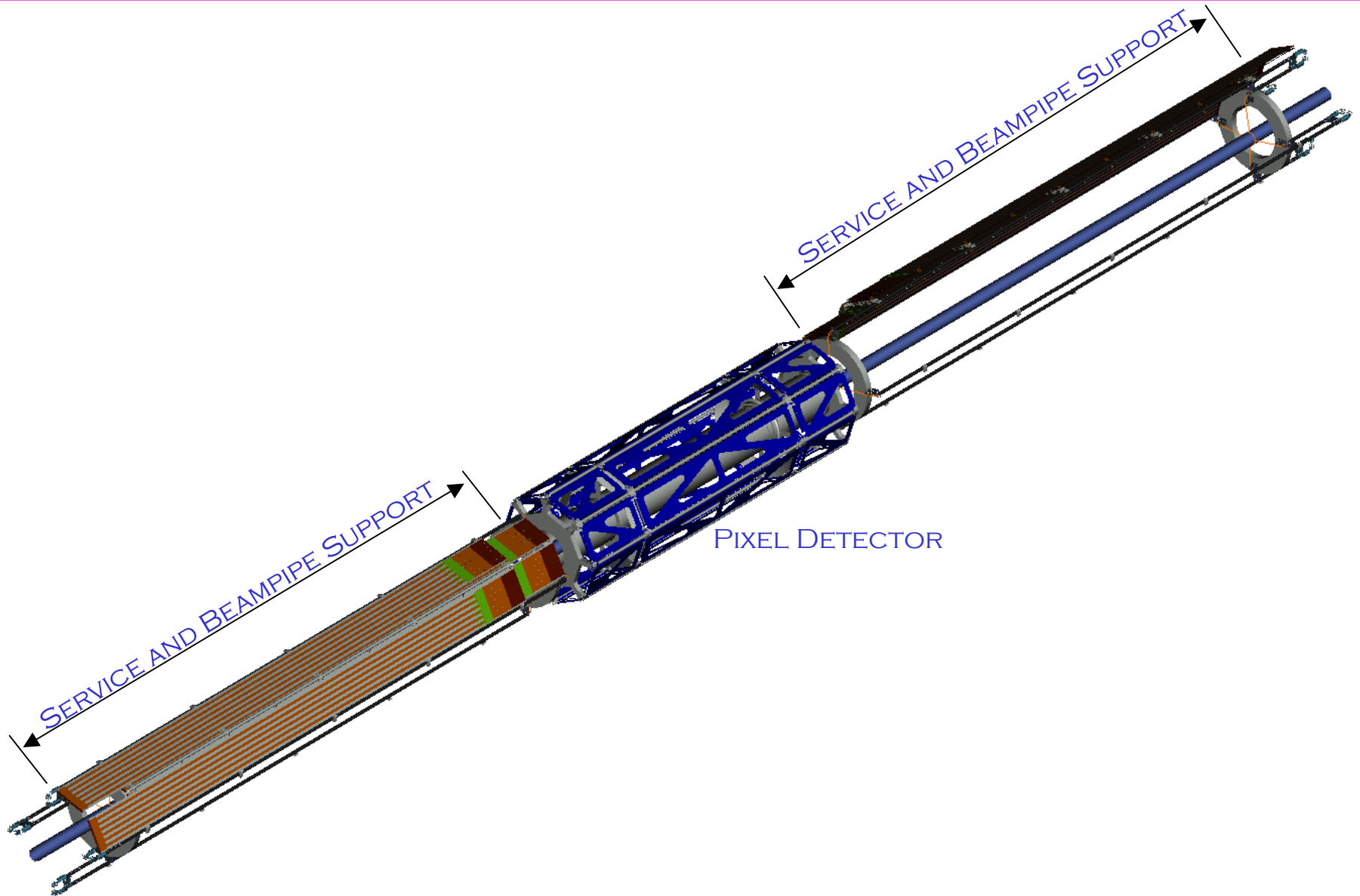
PIXEL SYSTEM AND BEAM PIPE WILL BE
ASSEMBLED ON THE SURFACE AND LOWERED
AS A PACKAGE INTO THE COLLISION HALL



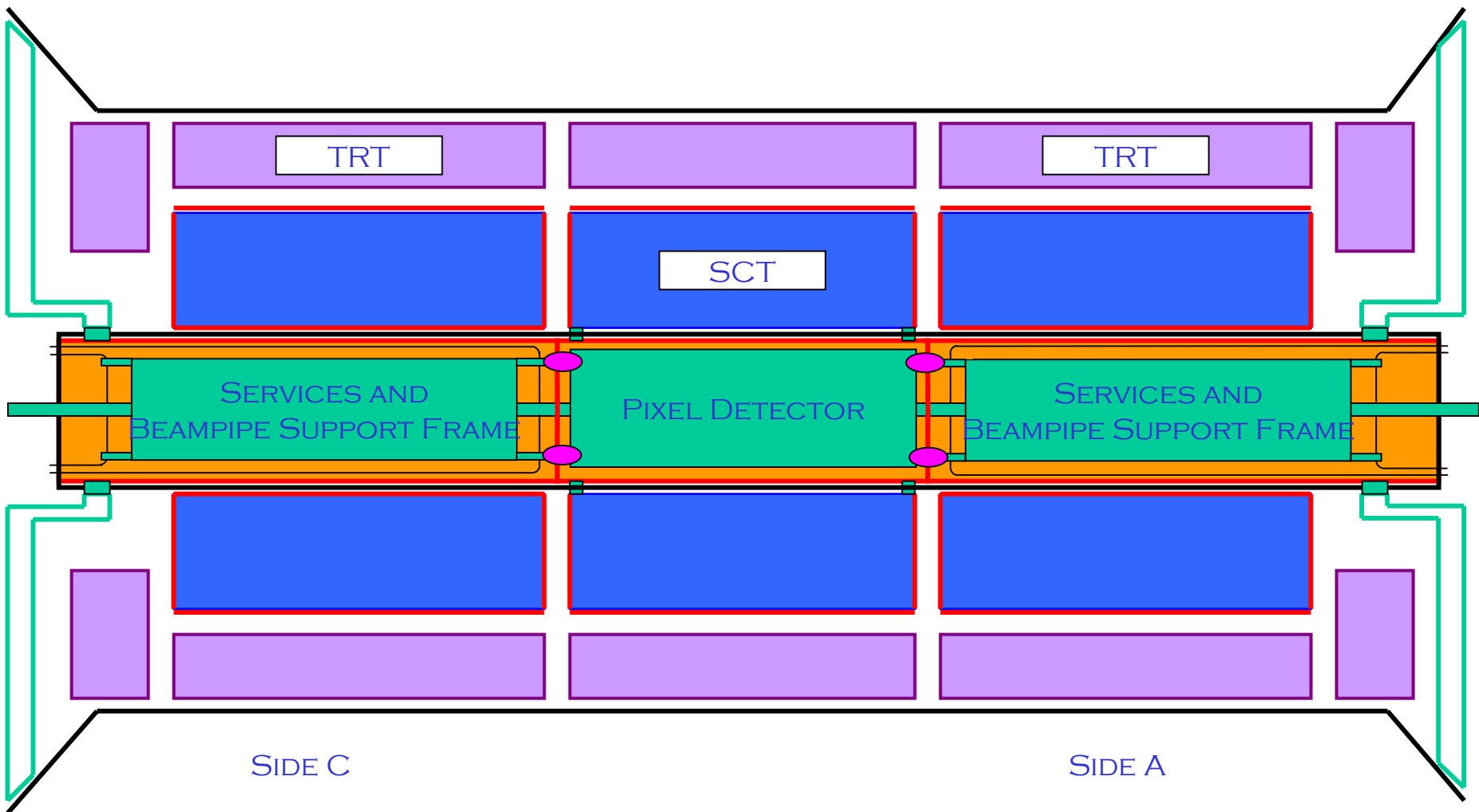
Pixel and Beam Pipe Assembly



Pixel and Beam Pipe Assembly



Pixels Installed



Pixel Mechanics

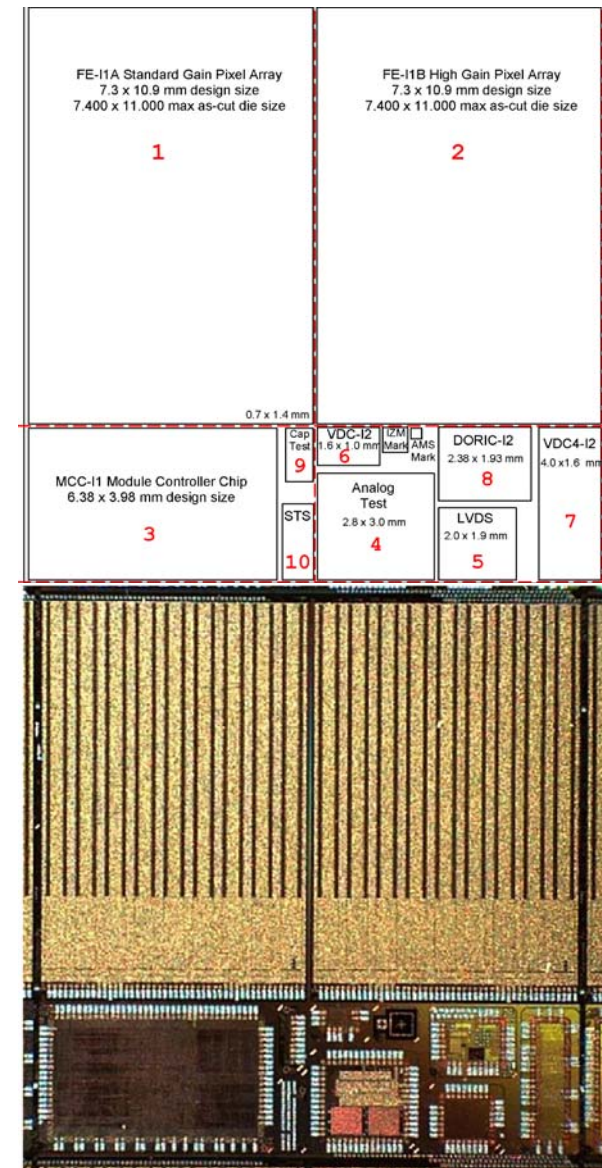
- We have started production of the disk sectors, which hold modules in the disk region, and this will be done this year(Wirth, Johnson, Weber).
- The first disk support ring will be completed this week, and production of the remainder will be done this year(external vendor).
- The design of the overall support frame is complete and we have gone out for bids for tooling and assembly. It will take about a year to complete.
- The conceptual design for the beam pipe support structure was reviewed at CERN two weeks ago. Prototype work is hoped to start in October, and production next year. The support will be assembled at LBNL from vendor supplied and in-house manufactured parts from our new composites facility established by the Eng. Div.(Anderssen, Hartman, Dardin)
- Prototypes of the Pixel Support Tube and related structures have been fabricated. The Support Tube, rails, service support panels and other composite structures will be manufactured primarily at LBNL starting in 2003. (Anderssen, Hartman, Dardin, Goozen, ME students)

Pixel Electronics

- History
 - Rad-soft ICs(HP) fabricated and tested extensively in lab and test beams. Proof-of-principle demonstrated already some years ago with prototype sensors and extensive beam tests. Efficiency, resolution goals met.
 - Conversion to rad-hard failed in DMILL(inadequate process for pixels) and Honeywell(financial)
 - Transition to 0.25 micron technology(IBM or TSMC) made for all integrated circuits needed for project. IBM is baseline, TSMC is backup(also for test chips).
- K. Einsweiler is overall ATLAS electronics coordinator.
- The strong LBNL IC group allows us to lead the pixel electronics effort(Blanquart, Denes, Mandelli, Meddeler)
- In addition, we are responsible for providing most of the IC and module tests systems for the collaboration, and these have also been designed and implemented by Einsweiler, Saavedra and LBNL engineers(Joseph, Richardson, Vu)

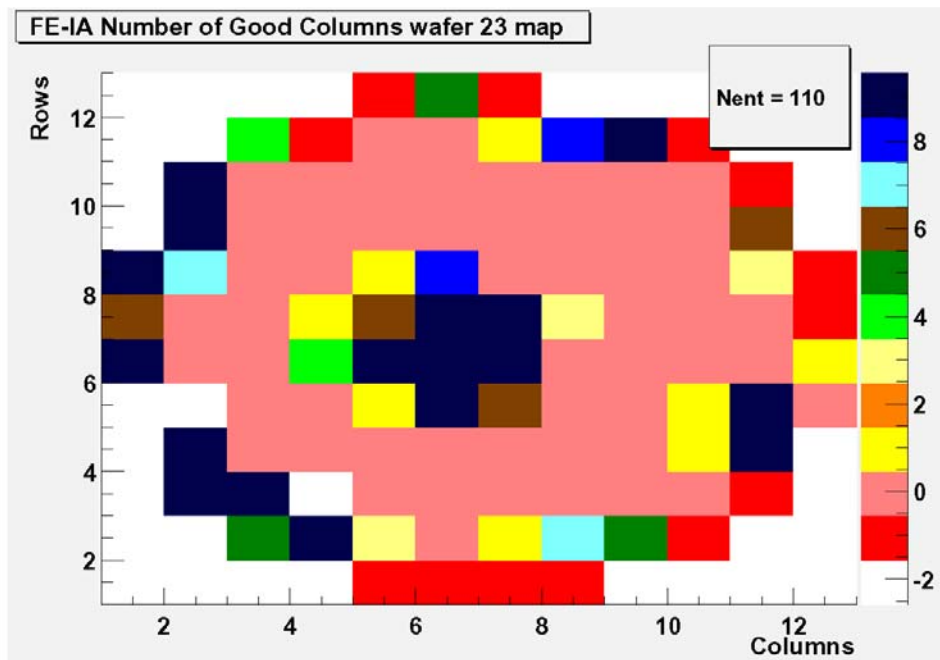
Pixel Integrated Circuits

- ICs Required
 - FE – front-end chip, 16 per pixel module
 - MCC – Module control chip, one per module
 - VDC and DORIC – optical receivers and driver chips for conversion of optical \leftrightarrow electrical signals
- Fabrication of the 1st full set of prototypes of these in the IBM 0.25 micron process was completed at the end of January.
- Preliminary testing complete, minor bugs found so far and yield is low.
- But sufficient to carry out complete irradiation and beam test program this summer!



Pixel IC Testing

- Typical wafer probe result for FE chips is shown below.
- Yield is low (about 15%) and pattern is clearly indicative of processing problem.
- Wafers have been returned for analysis to IBM, ongoing



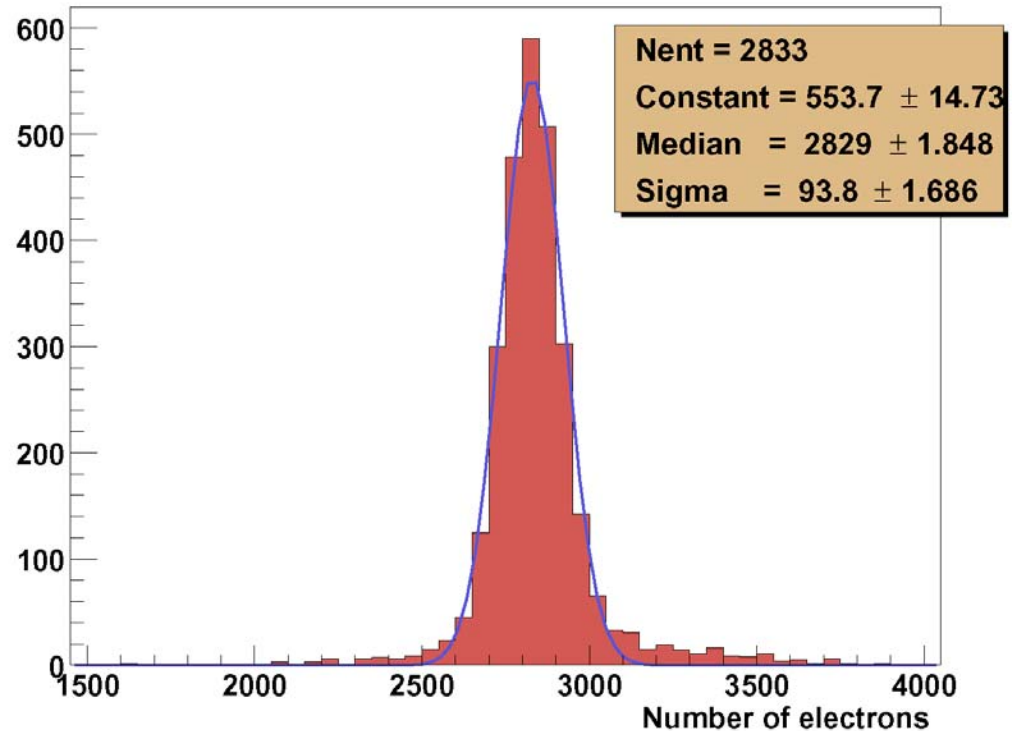
- Chips with no data appear White, bad Global Registers are Red, and other colors represent the Pixel Register test results. There are 18 (3) chips with working Global Registers and 9 (8) good column pairs in Pixel Register. This wafer was diced.

- IBM is making additional wafers (about 50) to help understand the problem.
- We will “swap” existing for new wafers shortly.

Pixel IC Testing

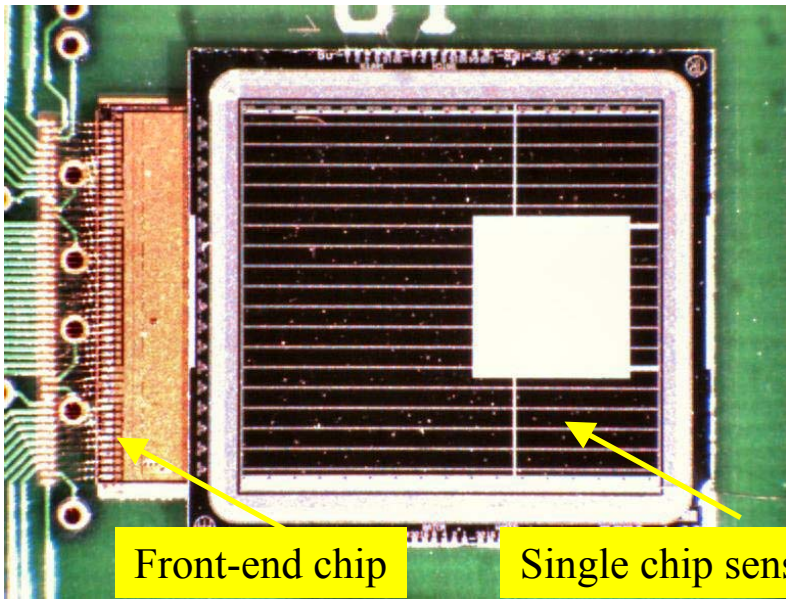
- Two FE chips have been irradiated at the LBNL 88" cyclotron to about 50 MRad. They worked during and after this irradiation. Previous test chips had been irradiated to over 100 MRad and still worked.
- The first assemblies of the FE chips with sensors were received a few weeks ago.
- Preliminary tests here indicate good functionality
- The first modules with these chips are about to arrive.

FE-IB: Threshold Distribution after 50MRad



- Any extensive irradiation program at CERN, followed by multiple test beam runs will occur this summer(Einsweiler, Richardson, Saavedra, Freeman, Blanquart).
- J. Richardson from here is coordinating the test beam effort for ATLAS and most of the hardware/software for the beam tests was done here.

Pixel Testing

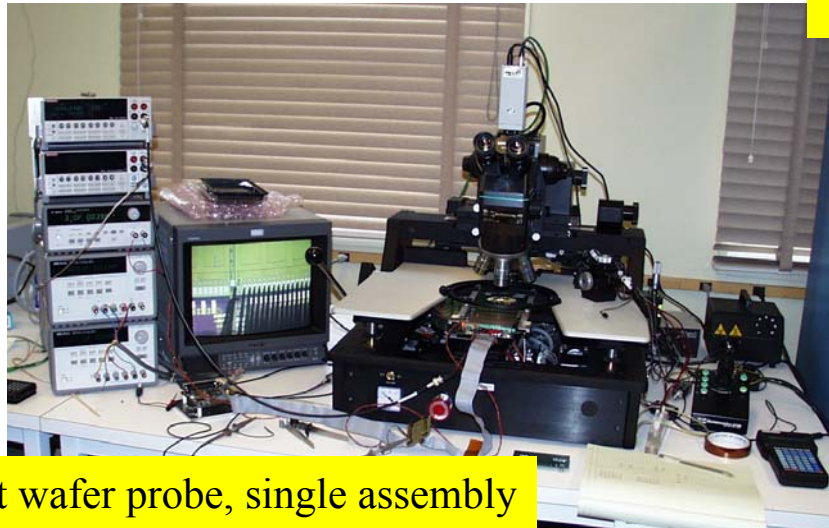


Front-end chip

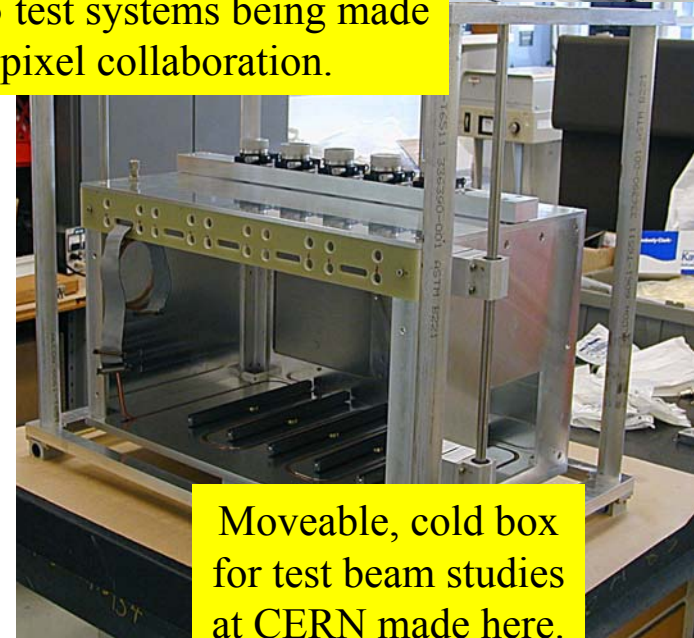
Single chip sensor



About 25 test systems being made for pixel collaboration.



Coherent wafer probe, single assembly module test system developed.



Moveable, cold box for test beam studies at CERN made here.

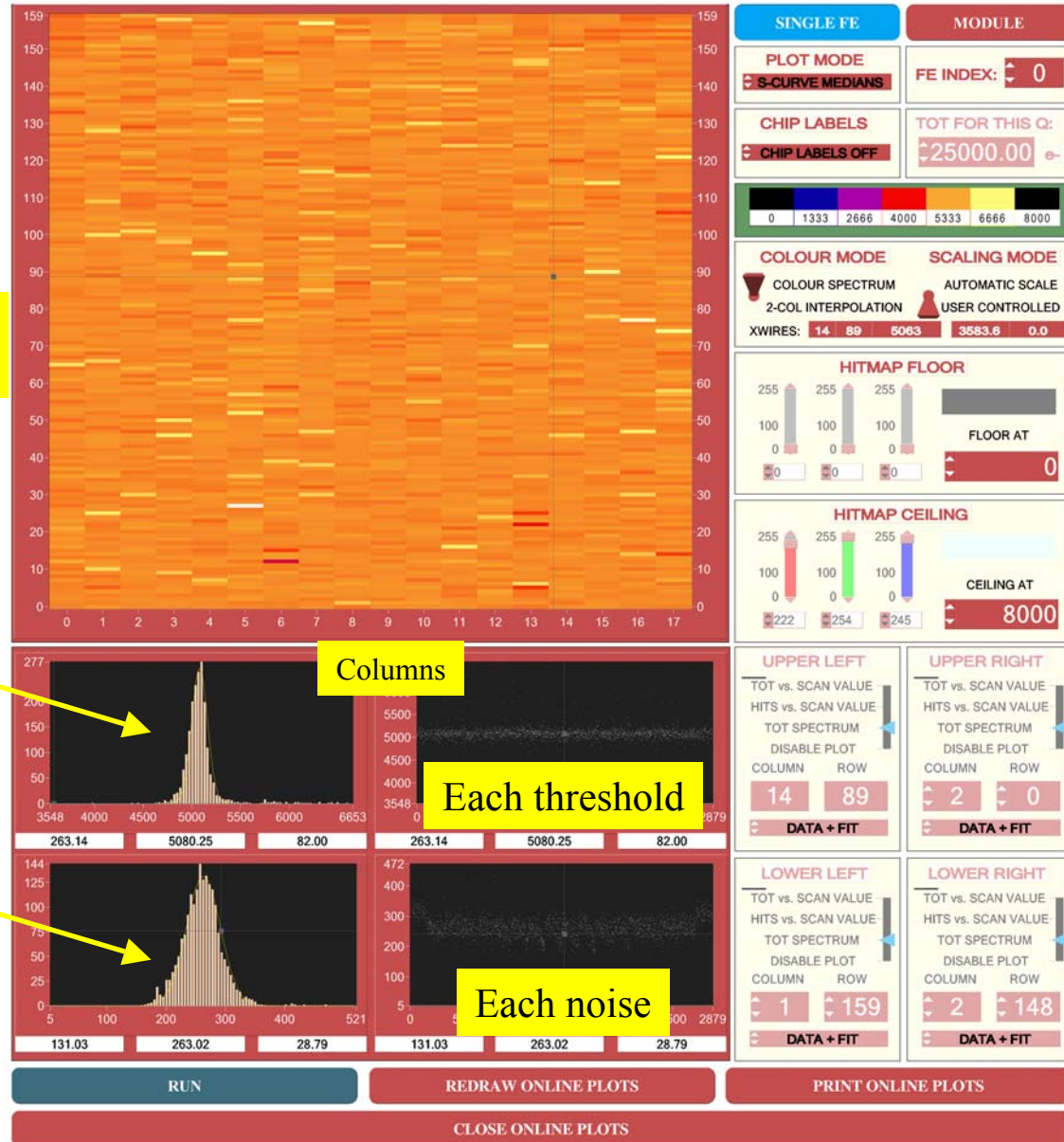
Screen Dump of Single Chip/Sensor

Hit map from
charge injection
showing thresholds

Rows

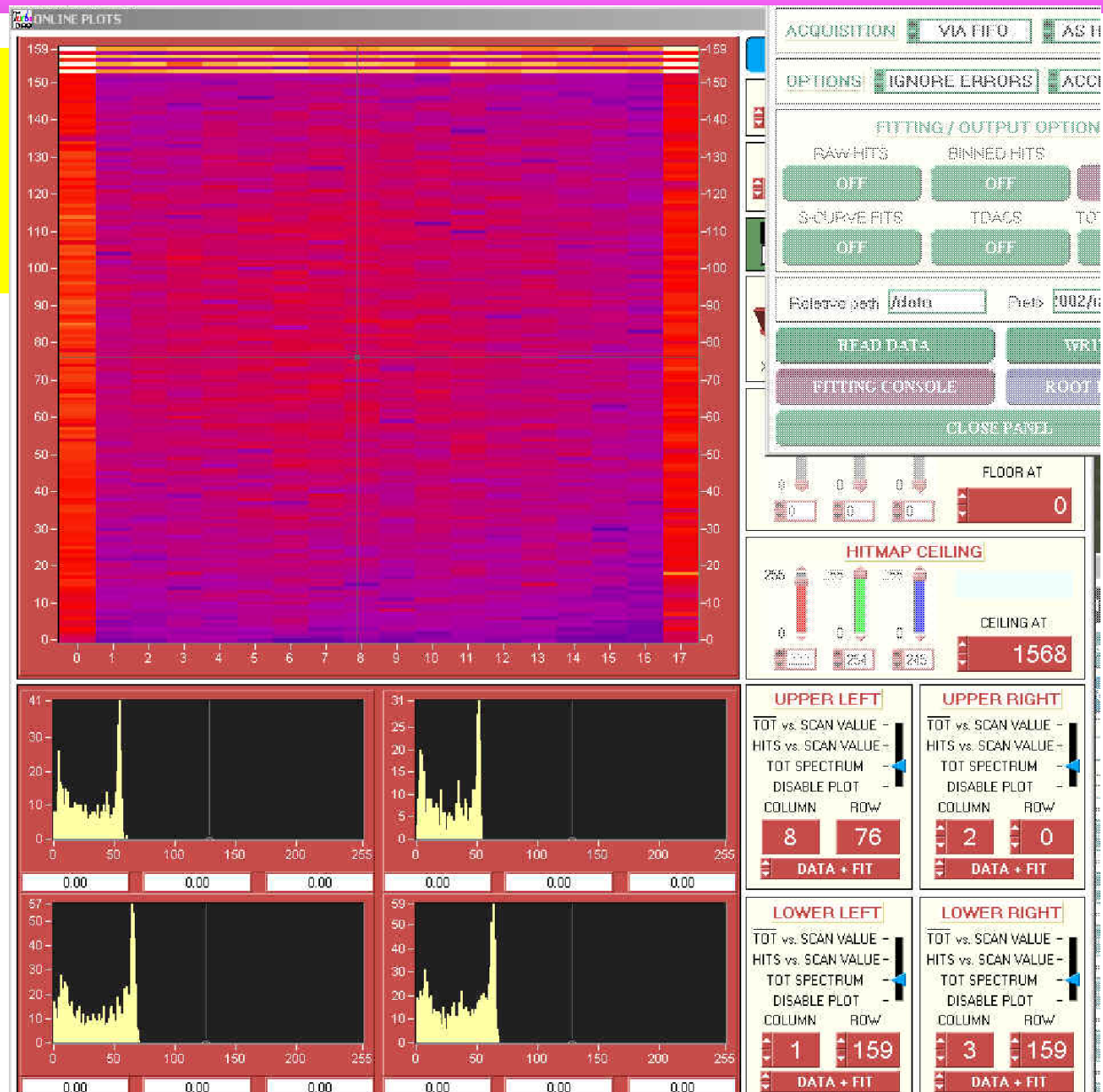
Pixel thresholds
after tuning(e's).
Mean is about 5080

Pixel noise(e's)
Mean is about 260



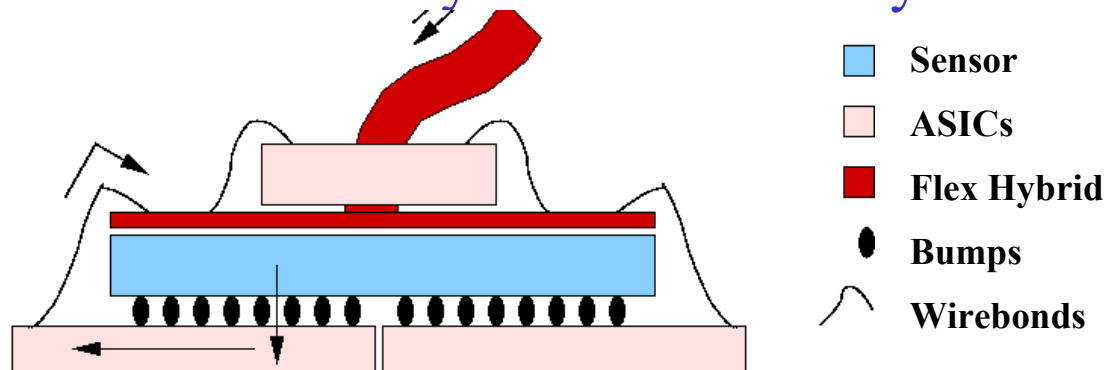
Source Measurement Different Assembly

Hit map showing charge from gamma source as measured by time-over-threshold in each pixel.

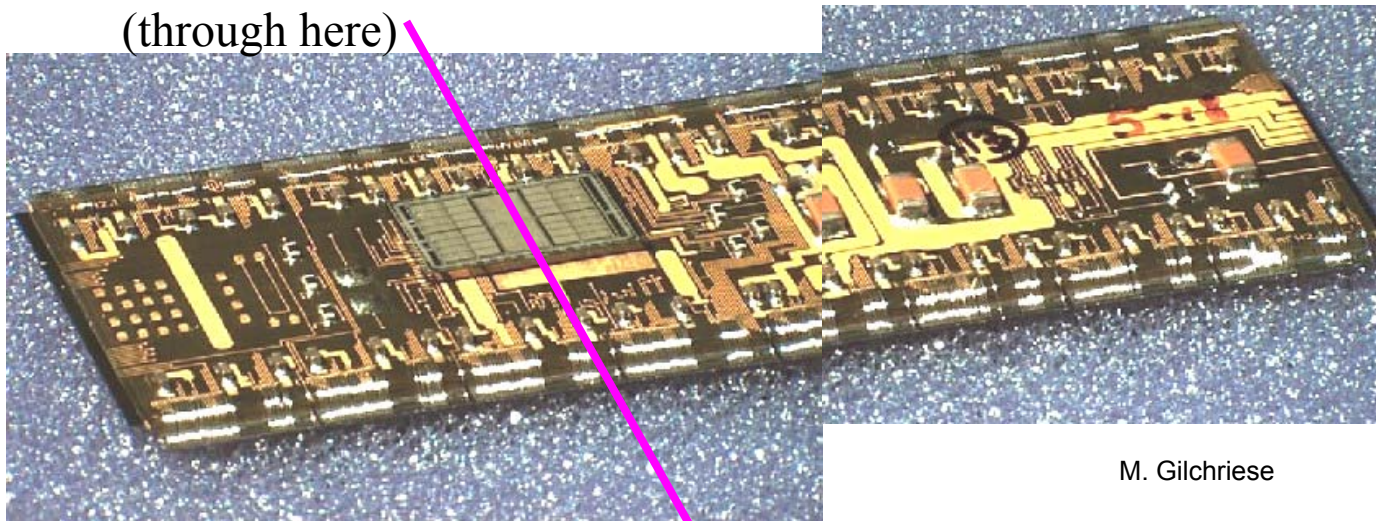


Pixel Hybrids and Modules

- M. Garcia-Sciveres has become the overall ATLAS module coordinator, which requires considerable interaction with other module assembly sites in Germany and Italy.

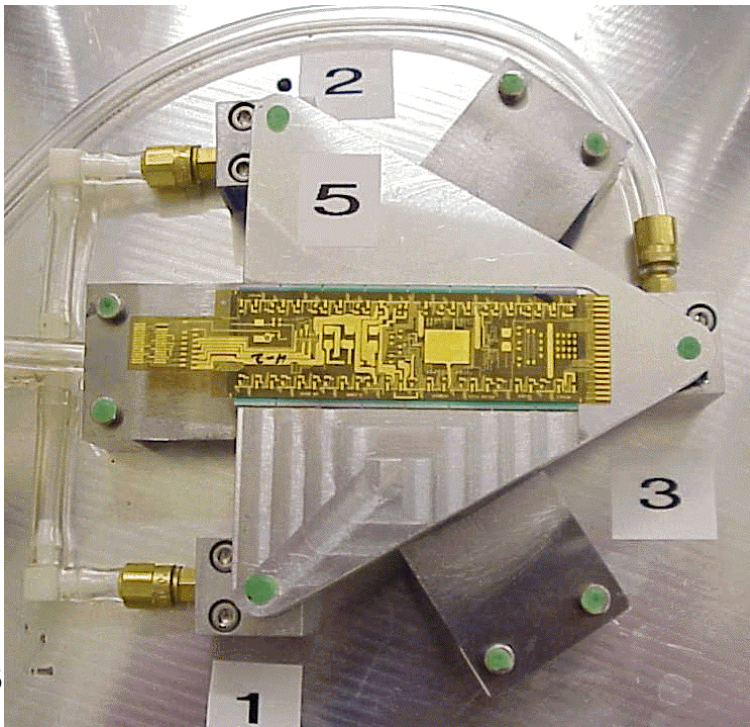


Schematic Cross Section
(through here)

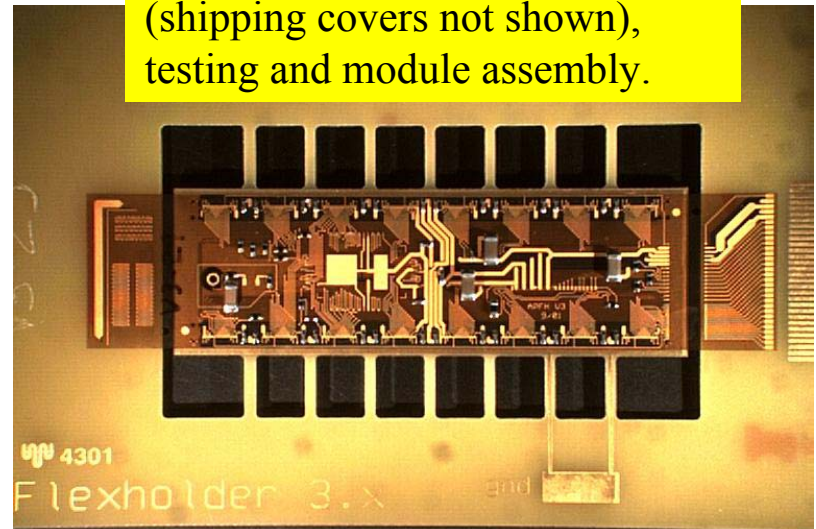


Module Assembly/Test

- Flex hybrids are fabricated and loaded, sent to LBNL(and other locations)
- Flip chip bonding of FE IC's to sensors done in Germany and Italy. “Bare modules” sent to LBNL(and other locations).
- Assembly, wire bonding and test of modules done here using tooling and procedures designed by Phys. Div. Engineer(Goozen).



Flex hybrid 3.x with components. Frame used for loading, transport (shipping covers not shown), testing and module assembly.



Pixel Plan

- Production sensors are now under fabrication and will be done by mid-2003
- Pixel mechanics partly in production, the rest starts next year.
- Next iteration of ICs this Fall after test beam program is evaluated.
- Will likely purchase additional wafers of existing chip set to push module production early(this has many steps that must be exercised).
- Electronics production starts summer 2003, followed by module construction.
- Module construction, placement on mechanics supports and local test in 2004.
- Action moves completely to CERN by early 2005, for surface assembly and test.

Towards the Research Program

- Planning for the so-called “research program” phase of ATLAS – preoperations, operations and maintenance, data taking and analysis – has started and is undergoing formal review.
- LBNL is expected to provide most of the technical support for the U.S. contributions to the pixel and SCT elements of this program, which would start in FY06. Although this seems like a long time away, we have to plan already now for this transition to retain key engineering and technical capabilities.
- We have proposed to begin R&D for replacement of pixel detector elements, starting with electronics R&D in FY04.
- Our experience tells us that it would be 5 years or more from starting R&D until one would be ready with a next-generation pixel detector suitable to replace what we are building now. Some elements of the pixel system will likely die on this timescale, and must be replaced.
- Supporting this early R&D will be challenge, since there will be intense competition for limited funding to finish ATLAS and begin operation.
- In years past, this type of R&D would have been jump-started by the Division, but clearly this is at risk given our dismal financial situation.

Concluding Remarks

- It's been a great year for progress on all aspects of our work on ATLAS!
- The efforts from our strong software and physics simulation team have matured and we can now turn our attention to the serious business of mock data challenges and final code.
- We have started the production phase for the silicon strip detector system.
- The first 0.25μ rad-hard prototypes of pixel electronics have been fabricated successfully and parts of the pixel system are now also in production.
- Our most significant immediate challenge is no longer technical but the financial health of the Physics Division.